

According to the present invention, the annular diffused region around the bipolar transistor 12 has a STI (Shallow Trench Isolation) structure to prevent the isolation area from forming a dishing portion after the CMP process.

Electrodes made of a silicide layer (CoSi_2) are formed on the annular diffused region, not for disposing thereon the interconnects. Interconnects are not disposed on the silicide layer in the operational final product, (see page 19, lines 5-19 in the present specification).

In support of this argument, please refer to Suzuki, U.S. Patent No. 6,265,747 B1, a copy of which is enclosed for the convenience of the Examiner. In Figs. 1F and 6K in Suzuki, an operational final structure of the bipolar transistor is shown only by specifying emitter/base/collector electrodes without their interconnects. Generally, as in Fig. 3C in Suzuki, the interconnect for connecting the annular diffused region with the semiconductor substrate is omitted. Such interconnect is specified in the specification or drawings only when it is necessary to describe a feature of the invention.

Similarly, the present specification and drawings do not show the interconnect for connecting the annular diffused region with the semiconductor substrate. Such description has been considered unnecessary since an early stage of the invention.

If interconnects for connecting the annular diffused region with the semiconductor substrate would be shown in addition to emitter/base/collector of the bipolar transistor, four interconnects would be necessary. If four interconnects were disposed on the silicide layer, in the present invention, the four interconnects would complicate the layout of the semiconductor, and obstruct design choice for the layout because the interconnects cannot be left floating without connections to each other.

Similarly, Seefeldt, U.S. Patent No. 6,355,537, cited in the Office Action, teaches the conductor 52 for connecting the metal contact 50 and the ground because it is necessary to describe the invention.

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hiramoto et al., (U.S. Patent No. 5,661,329), in view of Seefeldt. Claims 2-10 were rejected as being unpatentable under 35 U.S.C. §103(a) as being unpatentable over Hiramoto et al. and Seefeldt in view of Nii et al., (U.S. Patent No. 5,933,719).

Claim 1 provides that the annular diffused region has only one layer of material laid on top of an entirety of the annular diffused region. This feature is supported by page 21, lines 19-24, of the specification.

In contrast, in Seefeldt the metal contacts 50 are not formed on an entire region of the guard ring 36.

Attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Applicant submitted Information Disclosure Statements (IDS) herein on April 29, 2002 and October 15, 2002, but has not received Forms PTO-1449, which were attached to those IDS's to date. Applicant respectfully requests that such Forms PTO-1449 be sent with the next Office Action, appropriately initialed, signed, and dated.

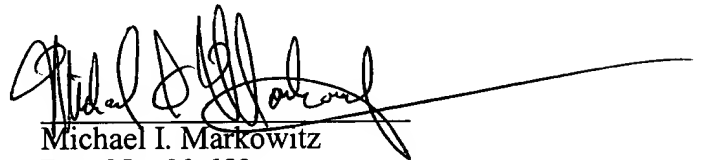
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made
Copy of Suzuki, U.S. Patent No. 6,265,747 B1

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claim 1 has been rewritten as follows:

1. (Thrice Amended) A semiconductor device comprising a silicon substrate, and a bipolar transistor having a collector well having a first conductivity-type, an internal base region having a second conductivity-type and received in said collector well and an emitter region having said first conductivity-type and received in said internal base region, a first annular isolation trench encircling said collector well, a second annular isolation trench encircling said first annular isolation trench, and an annular diffused region having said second conductivity-type disposed between said first annular isolation trench and said second annular isolation trench while being in contact with said first and second annular isolation trenches, said annular diffused region having only one layer of material laid on top of an entirety of said annular diffused region.